FIG. 1

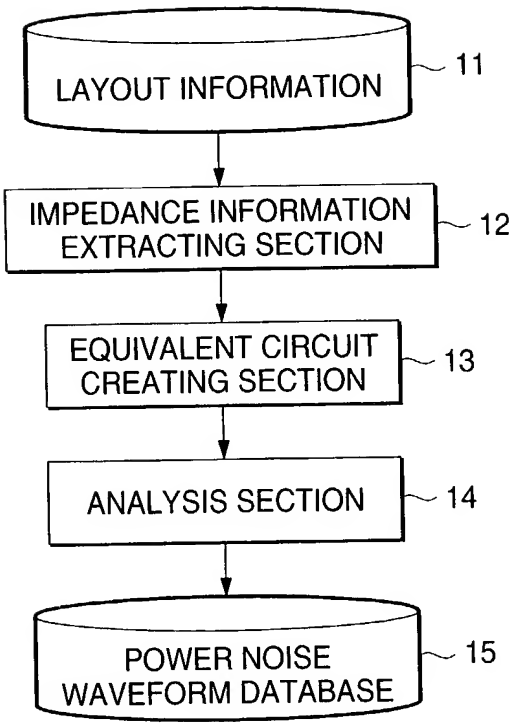
LAYOUT INFORMATION
11
IMPEDANCE INFORMATION EXTRACTING SECTION
12
EQUIVALENT CIRCUIT CREATING SECTION
13
ANALYSIS SECTION
14
POWER NOISE WAVEFORM DATABASE
15

FIG. 2A

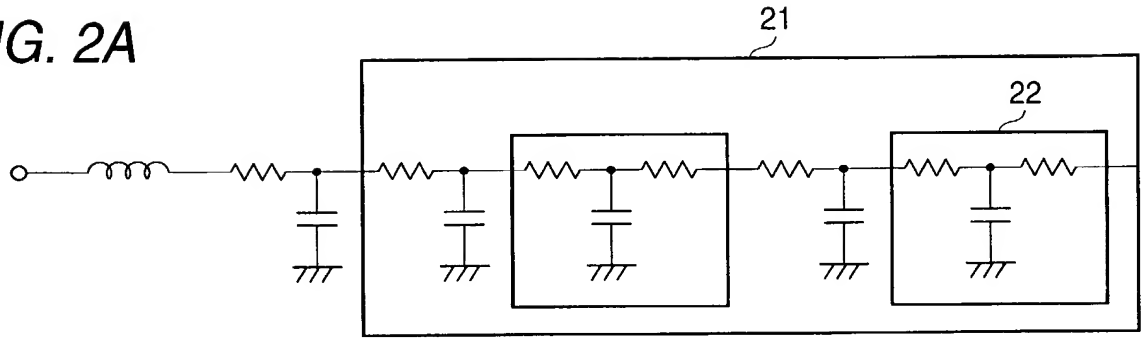

FIG. 2B

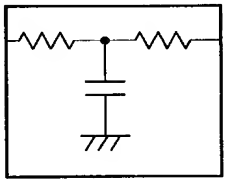

FIG. 2C

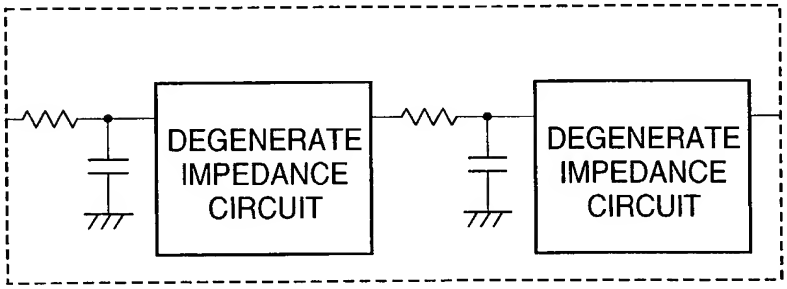

FIG. 2D

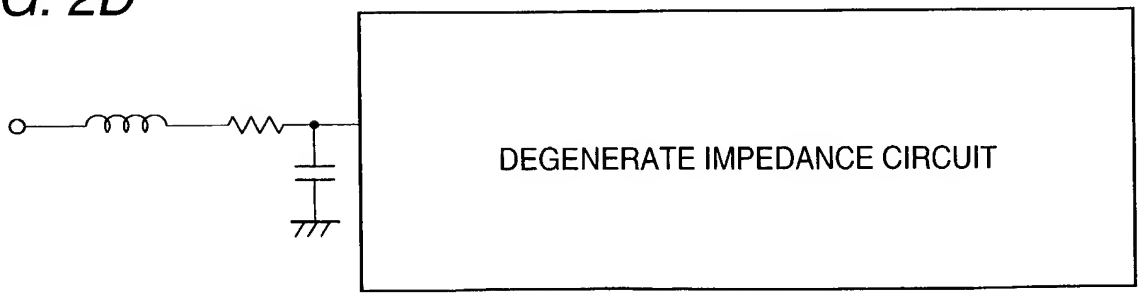

FIG. 3

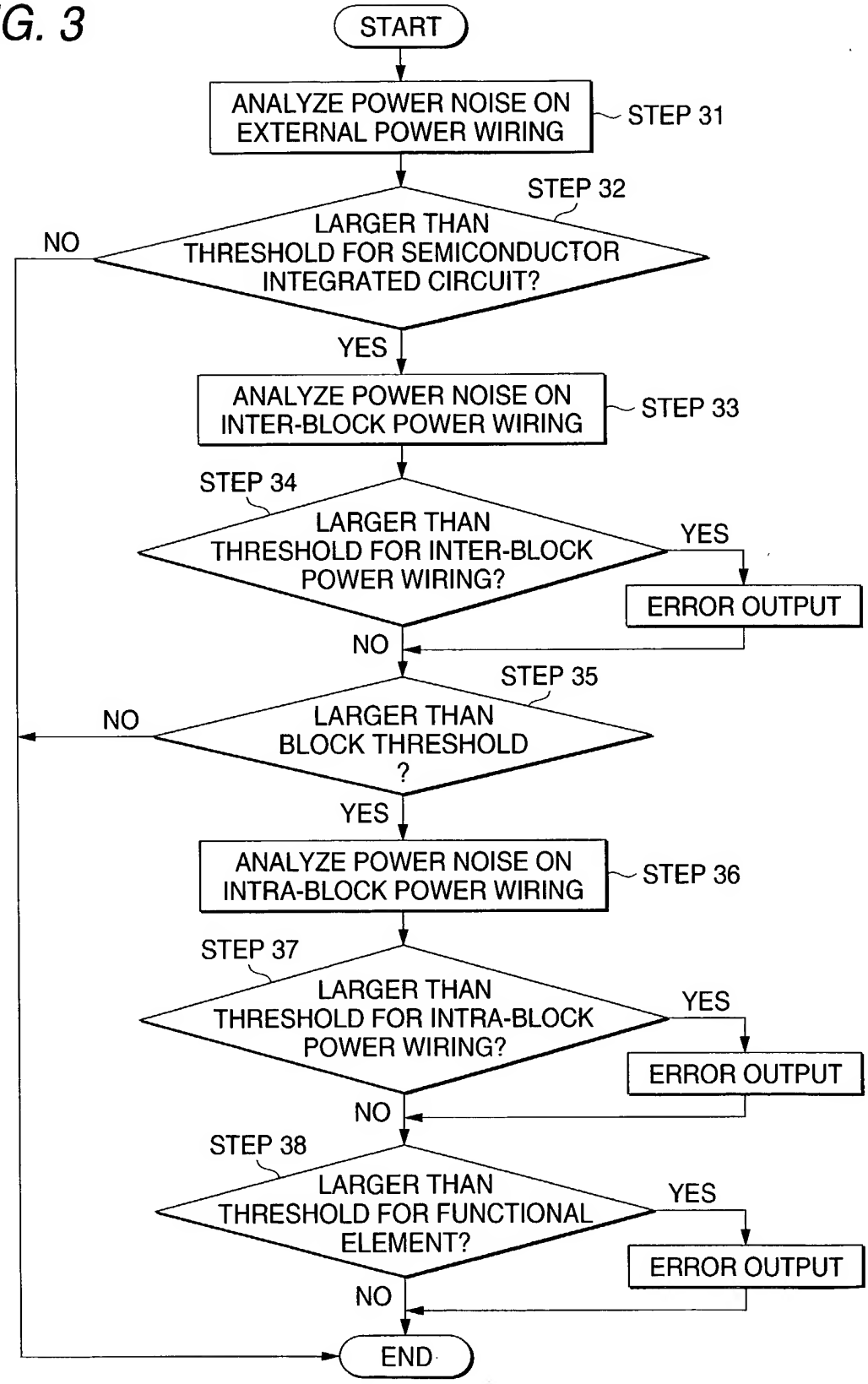
START
ANALYZE POWER NOISE ON EXTERNAL POWER WIRING
STEP 31
STEP 32
LARGER THAN THRESHOLD FOR SEMICONDUCTOR INTEGRATED CIRCUIT?
NO
YES
ANALYZE POWER NOISE ON INTER-BLOCK POWER WIRING
STEP 33
STEP 34
LARGER THAN THRESHOLD FOR INTER-BLOCK POWER WIRING?
YES
ERROR OUTPUT
NO
STEP 35
LARGER THAN BLOCK THRESHOLD ?
NO
YES
ANALYZE POWER NOISE ON INTRA-BLOCK POWER WIRING
STEP 36
STEP 37
LARGER THAN THRESHOLD FOR INTRA-BLOCK POWER WIRING?
YES
ERROR OUTPUT
NO
STEP 38
LARGER THAN THRESHOLD FOR FUNCTIONAL ELEMENT?
YES
ERROR OUTPUT
NO
END

FIG. 4

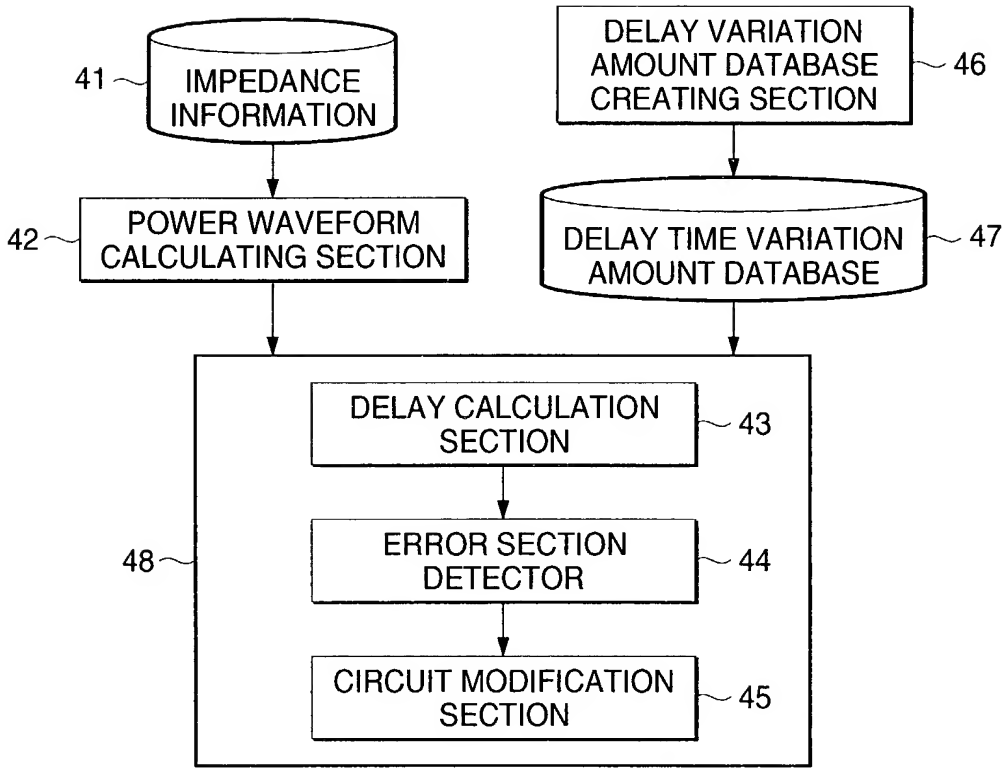
41
IMPEDANCE INFORMATION
42
POWER WAVEFORM CALCULATING SECTION
DELAY VARIATION AMOUNT DATABASE CREATING SECTION
46
DELAY TIME VARIATION AMOUNT DATABASE
47
48
DELAY CALCULATION SECTION
43
ERROR SECTION DETECTOR
44
CIRCUIT MODIFICATION SECTION
45

FIG. 5

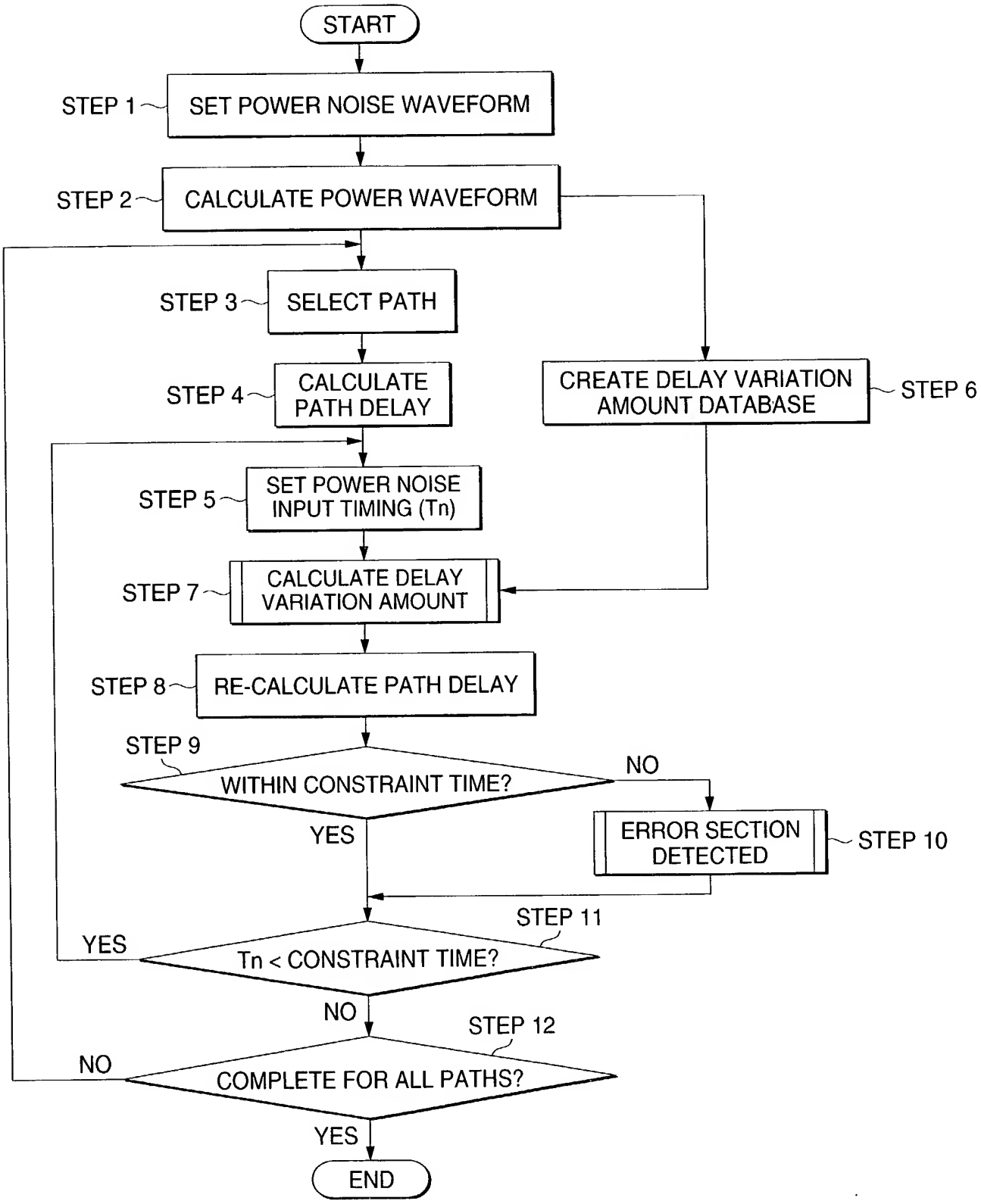
START
STEP 1
SET POWER NOISE WAVEFORM
STEP 2
CALCULATE POWER WAVEFORM
STEP 3
SELECT PATH
STEP 4
CALCULATE PATH DELAY
CREATE DELAY VARIATION AMOUNT DATABASE
STEP 6
STEP 5
SET POWER NOISE INPUT TIMING (Tn)
STEP 7
CALCULATE DELAY VARIATION AMOUNT
STEP 8
RE-CALCULATE PATH DELAY
STEP 9
WITHIN CONSTRAINT TIME?
NO
YES
ERROR SECTION DETECTED
STEP 10
STEP 11
YES
Tn < CONSTRAINT TIME?
NO
STEP 12
NO
COMPLETE FOR ALL PATHS?
YES
END

FIG. 6

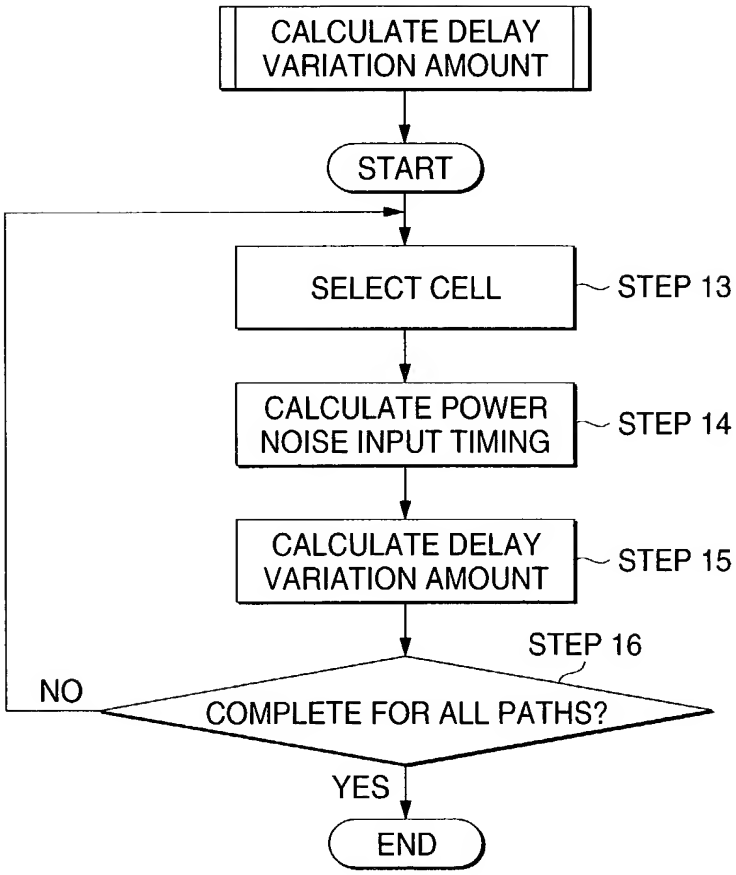
CALCULATE DELAY VARIATION AMOUNT
START
SELECT CELL
STEP 13
CALCULATE POWER NOISE INPUT TIMING
STEP 14
CALCULATE DELAY VARIATION AMOUNT
STEP 15
STEP 16
NO
COMPLETE FOR ALL PATHS?
YES
END

FIG. 7

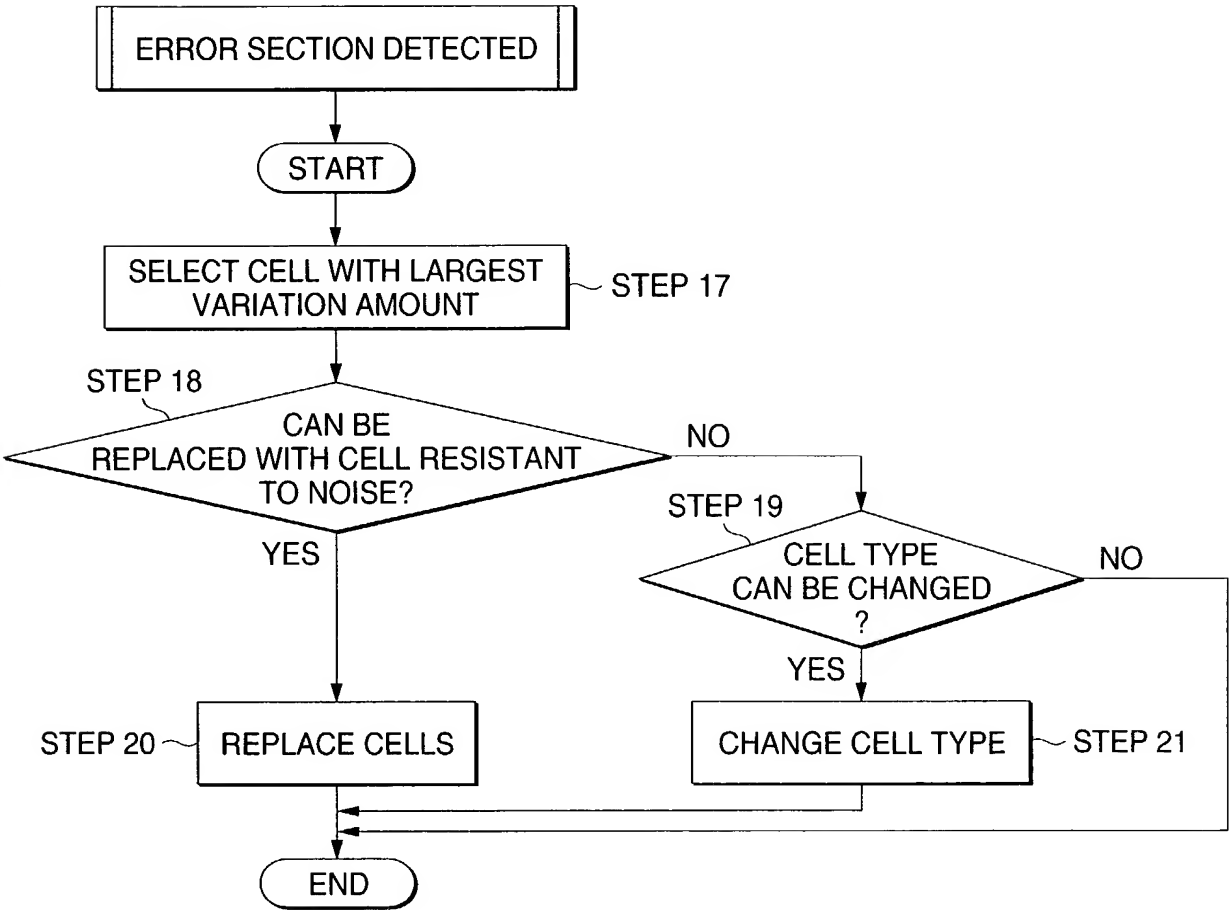

FIG. 8

CELL NAME	PEAK VALUE	DELAY VARIATION AMOUNT PER POWER NOISE INPUT TIMING				
		-20	-10	0	+10	+20
NAND1	10	0	-3	-5	-3	0
NAND1	5	0	-1	-3	-1	0
NAND1	-5	0	+1	+3	+1	0
NAND1	-10	0	+3	+5	+3	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮

FIG. 9A

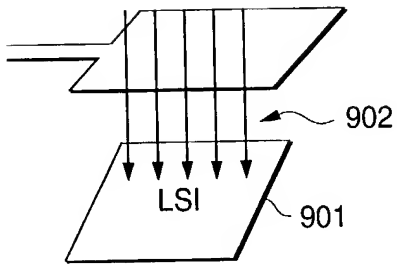

FIG. 9B

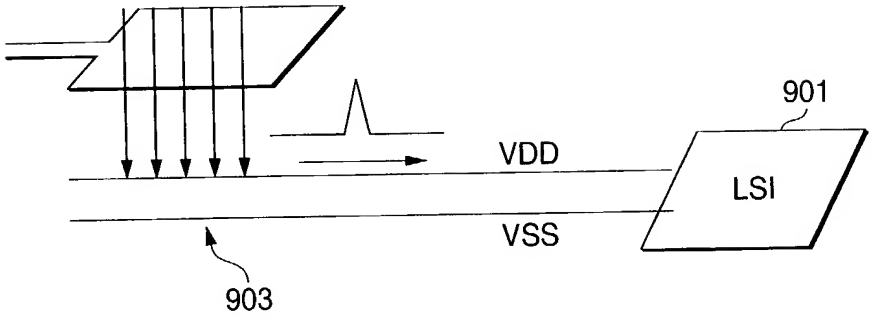

FIG. 10

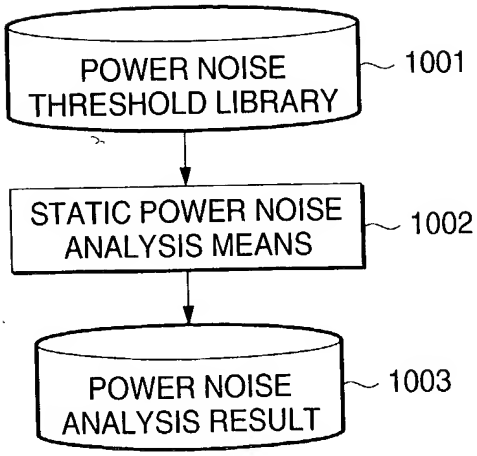

FIG. 11A

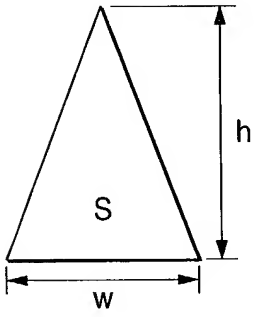

FIG. 11B

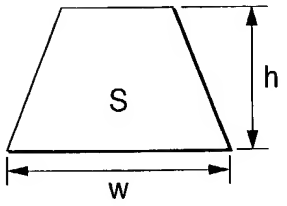

FIG. 11C

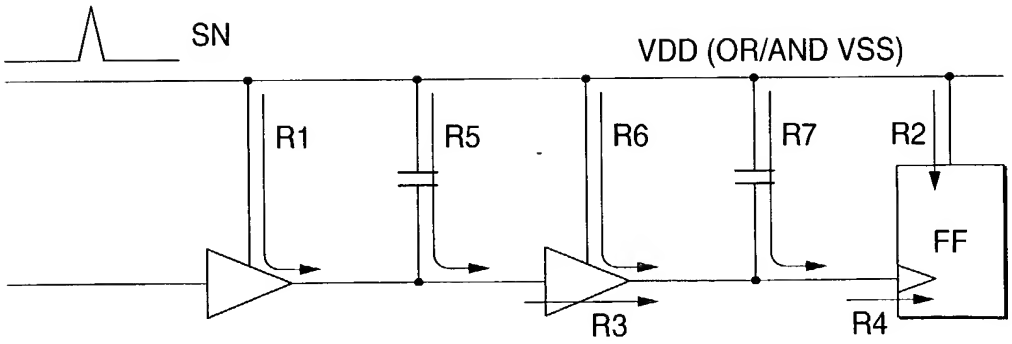

FIG. 12

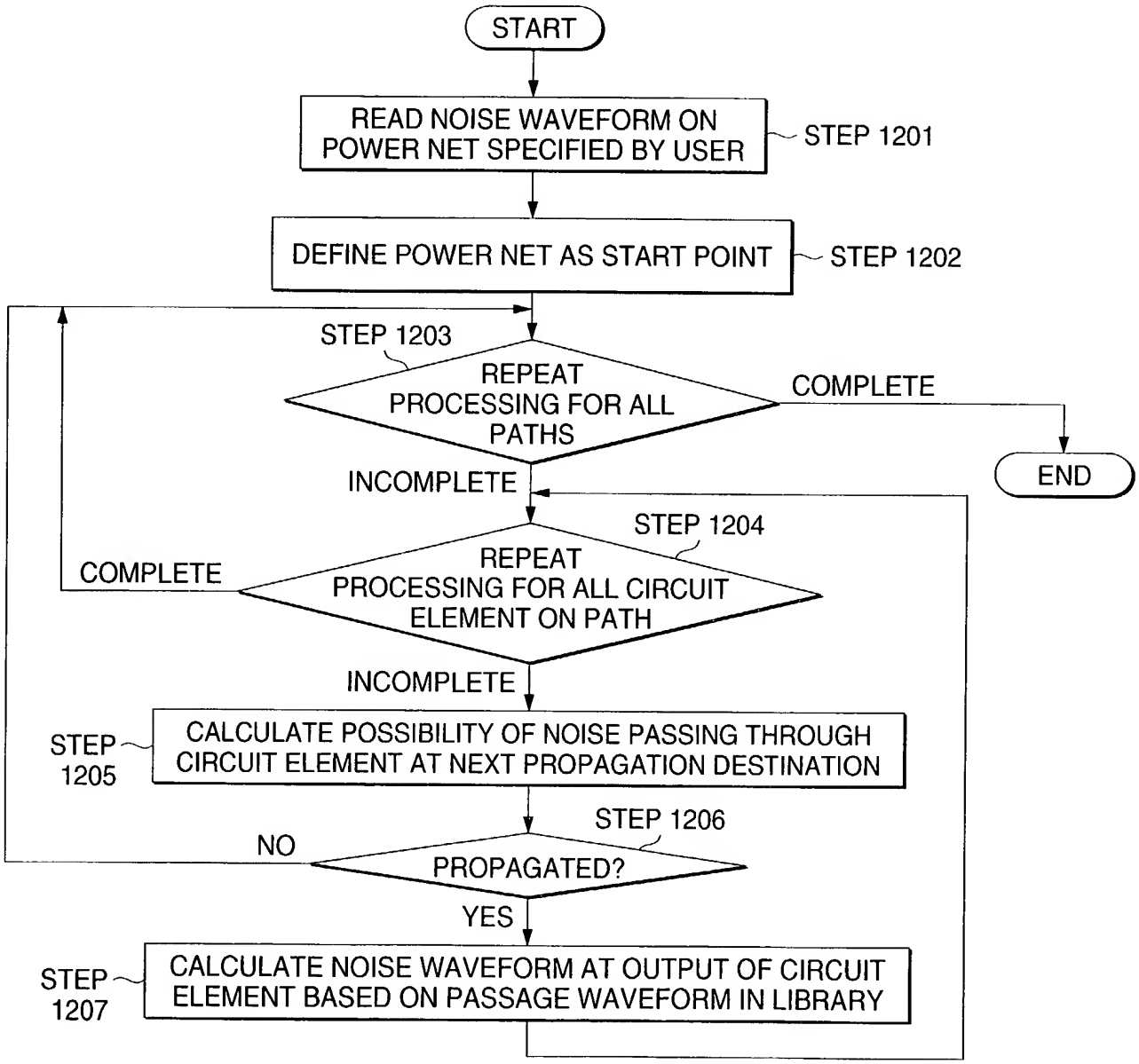
START
READ NOISE WAVEFORM ON POWER NET SPECIFIED BY USER
STEP 1201
DEFINE POWER NET AS START POINT
STEP 1202
STEP 1203
REPEAT PROCESSING FOR ALL PATHS
COMPLETE
END
INCOMPLETE
STEP 1204
REPEAT PROCESSING FOR ALL CIRCUIT ELEMENT ON PATH
COMPLETE
INCOMPLETE
STEP 1205
CALCULATE POSSIBILITY OF NOISE PASSING THROUGH CIRCUIT ELEMENT AT NEXT PROPAGATION DESTINATION
STEP 1206
NO
PROPAGATED?
YES
STEP 1207
CALCULATE NOISE WAVEFORM AT OUTPUT OF CIRCUIT ELEMENT BASED ON PASSAGE WAVEFORM IN LIBRARY

FIG. 13

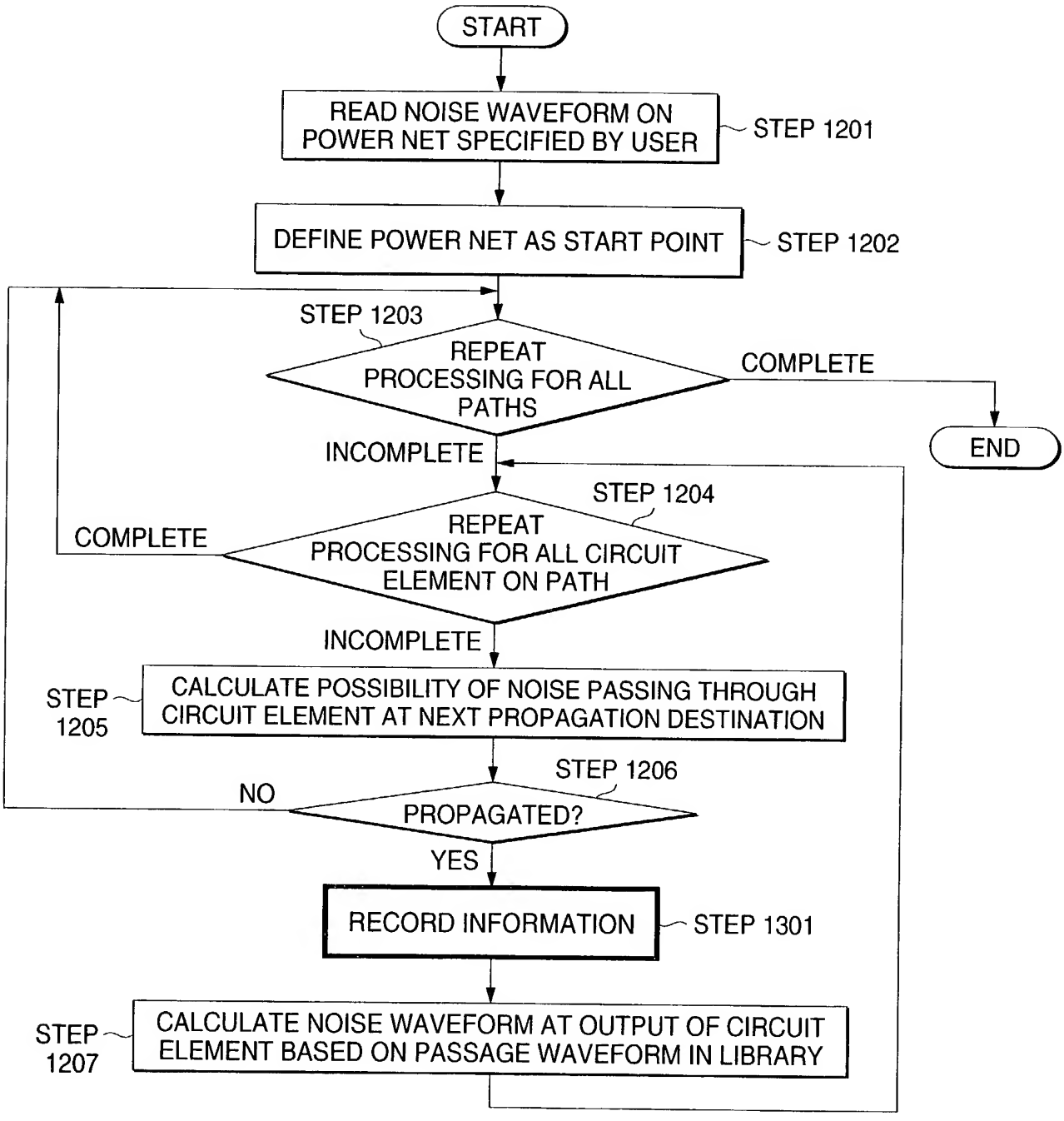
START
READ NOISE WAVEFORM ON POWER NET SPECIFIED BY USER
STEP 1201
DEFINE POWER NET AS START POINT
STEP 1202
STEP 1203
REPEAT PROCESSING FOR ALL PATHS
COMPLETE
END
INCOMPLETE
STEP 1204
REPEAT PROCESSING FOR ALL CIRCUIT ELEMENT ON PATH
COMPLETE
INCOMPLETE
STEP 1205
CALCULATE POSSIBILITY OF NOISE PASSING THROUGH CIRCUIT ELEMENT AT NEXT PROPAGATION DESTINATION
STEP 1206
NO
PROPAGATED?
YES
RECORD INFORMATION
STEP 1301
STEP 1207
CALCULATE NOISE WAVEFORM AT OUTPUT OF CIRCUIT ELEMENT BASED ON PASSAGE WAVEFORM IN LIBRARY

FIG. 14

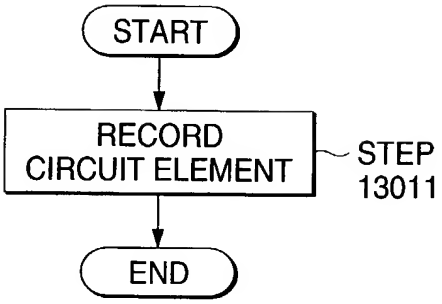

FIG. 15

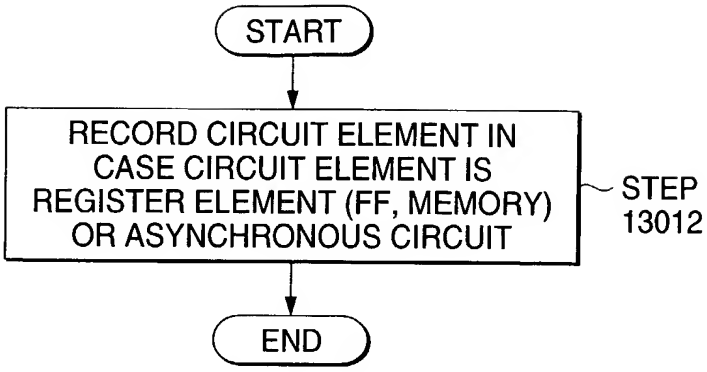

FIG. 16

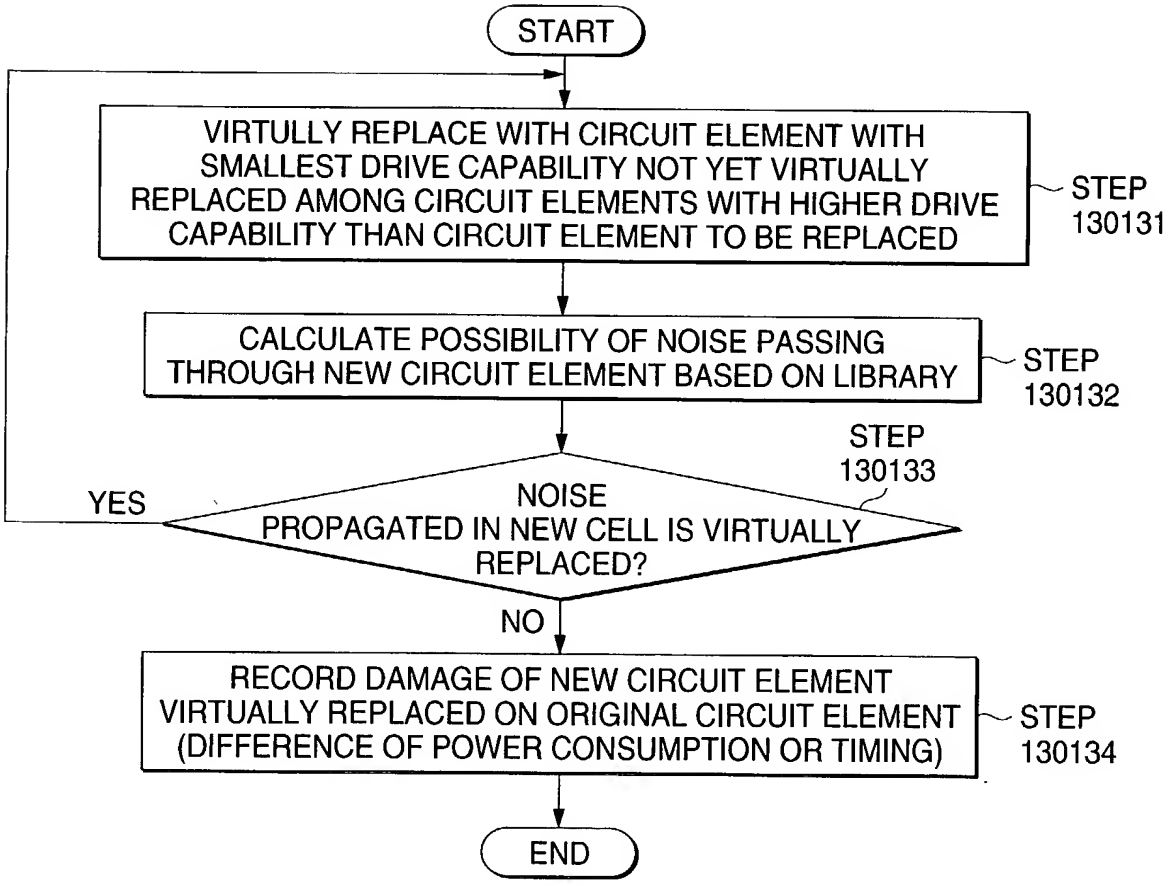

FIG. 17

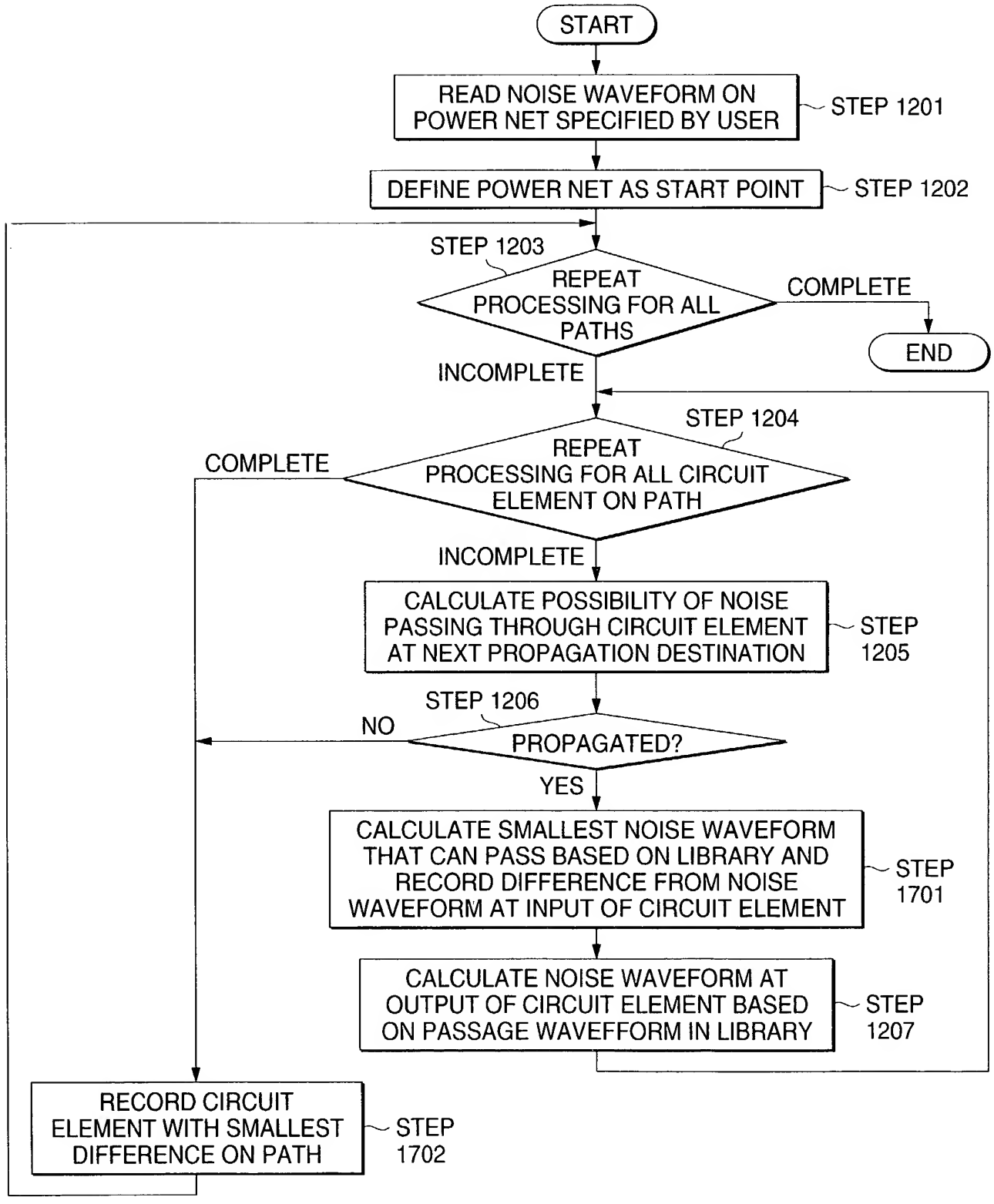
START
READ NOISE WAVEFORM ON POWER NET SPECIFIED BY USER
STEP 1201
DEFINE POWER NET AS START POINT
STEP 1202
STEP 1203
REPEAT PROCESSING FOR ALL PATHS
COMPLETE
END
INCOMPLETE
STEP 1204
REPEAT PROCESSING FOR ALL CIRCUIT ELEMENT ON PATH
COMPLETE
INCOMPLETE
CALCULATE POSSIBILITY OF NOISE PASSING THROUGH CIRCUIT ELEMENT AT NEXT PROPAGATION DESTINATION
STEP 1205
STEP 1206
NO
PROPAGATED?
YES
CALCULATE SMALLEST NOISE WAVEFORM THAT CAN PASS BASED ON LIBRARY AND RECORD DIFFERENCE FROM NOISE WAVEFORM AT INPUT OF CIRCUIT ELEMENT
STEP 1701
CALCULATE NOISE WAVEFORM AT OUTPUT OF CIRCUIT ELEMENT BASED ON PASSAGE WAVEFFORM IN LIBRARY
STEP 1207
RECORD CIRCUIT ELEMENT WITH SMALLEST DIFFERENCE ON PATH
STEP 1702

FIG. 18

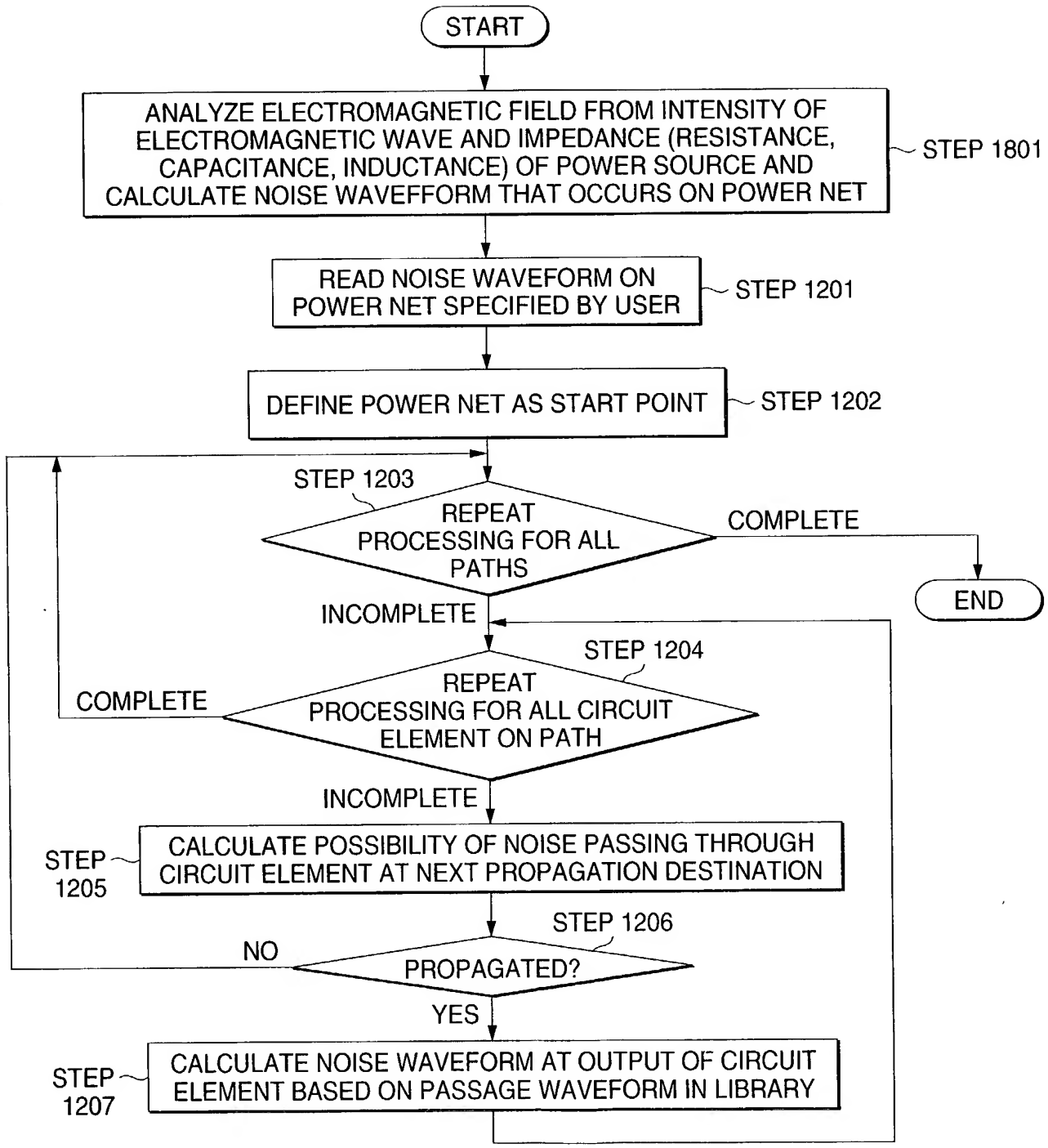
START
ANALYZE ELECTROMAGNETIC FIELD FROM INTENSITY OF ELECTROMAGNETIC WAVE AND IMPEDANCE (RESISTANCE, CAPACITANCE, INDUCTANCE) OF POWER SOURCE AND CALCULATE NOISE WAVEFFORM THAT OCCURS ON POWER NET
STEP 1801
READ NOISE WAVEFORM ON POWER NET SPECIFIED BY USER
STEP 1201
DEFINE POWER NET AS START POINT
STEP 1202
STEP 1203
REPEAT PROCESSING FOR ALL PATHS
COMPLETE
END
INCOMPLETE
STEP 1204
REPEAT PROCESSING FOR ALL CIRCUIT ELEMENT ON PATH
COMPLETE
INCOMPLETE
STEP 1205
CALCULATE POSSIBILITY OF NOISE PASSING THROUGH CIRCUIT ELEMENT AT NEXT PROPAGATION DESTINATION
STEP 1206
NO
PROPAGATED?
YES
STEP 1207
CALCULATE NOISE WAVEFORM AT OUTPUT OF CIRCUIT ELEMENT BASED ON PASSAGE WAVEFORM IN LIBRARY

FIG. 19

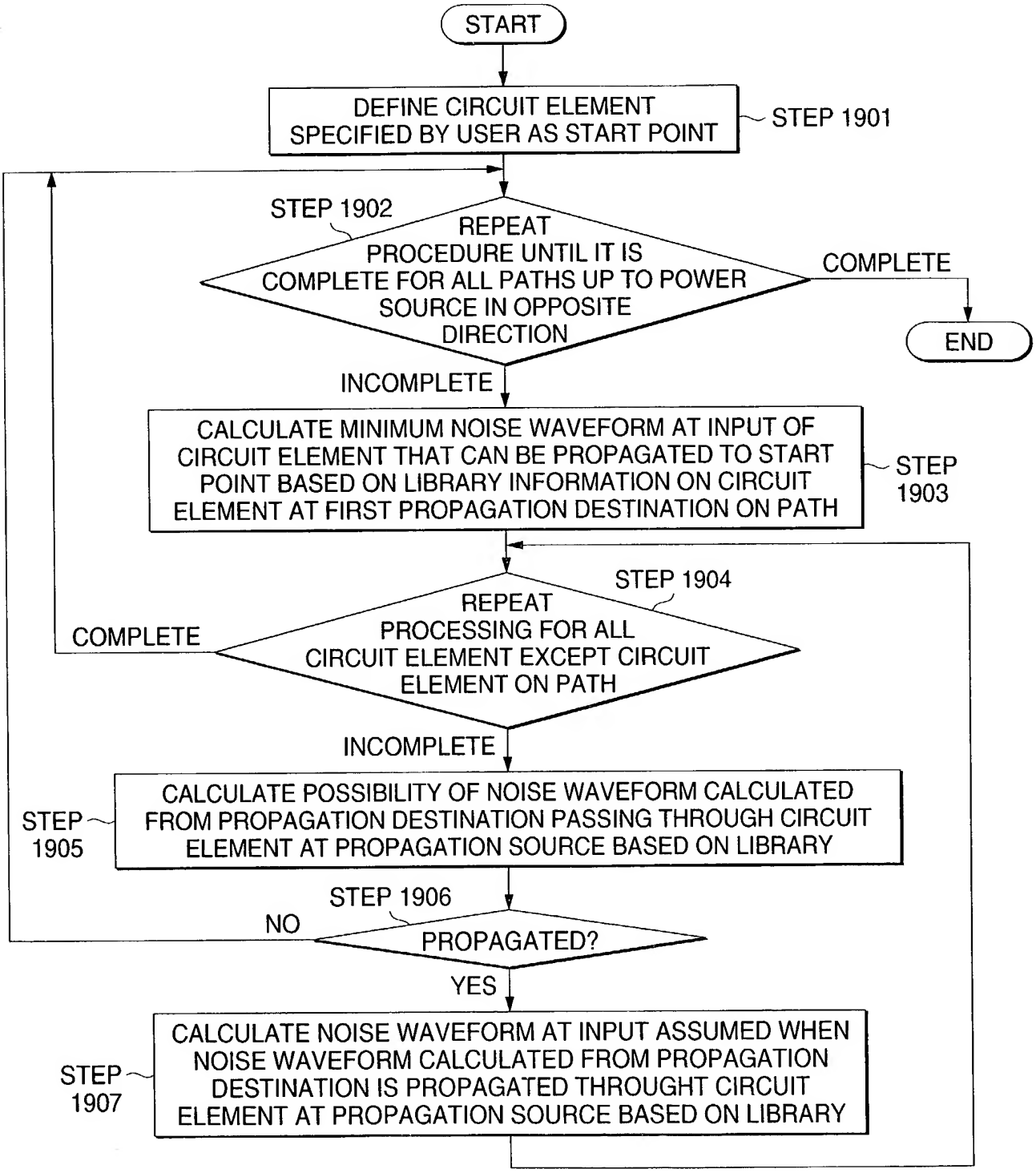
START
DEFINE CIRCUIT ELEMENT SPECIFIED BY USER AS START POINT
STEP 1901
STEP 1902
REPEAT PROCEDURE UNTIL IT IS COMPLETE FOR ALL PATHS UP TO POWER SOURCE IN OPPOSITE DIRECTION
COMPLETE
END
INCOMPLETE
CALCULATE MINIMUM NOISE WAVEFORM AT INPUT OF CIRCUIT ELEMENT THAT CAN BE PROPAGATED TO START POINT BASED ON LIBRARY INFORMATION ON CIRCUIT ELEMENT AT FIRST PROPAGATION DESTINATION ON PATH
STEP 1903
STEP 1904
REPEAT PROCESSING FOR ALL CIRCUIT ELEMENT EXCEPT CIRCUIT ELEMENT ON PATH
COMPLETE
INCOMPLETE
STEP 1905
CALCULATE POSSIBILITY OF NOISE WAVEFORM CALCULATED FROM PROPAGATION DESTINATION PASSING THROUGH CIRCUIT ELEMENT AT PROPAGATION SOURCE BASED ON LIBRARY
STEP 1906
NO
PROPAGATED?
YES
STEP 1907
CALCULATE NOISE WAVEFORM AT INPUT ASSUMED WHEN NOISE WAVEFORM CALCULATED FROM PROPAGATION DESTINATION IS PROPAGATED THROUGHT CIRCUIT ELEMENT AT PROPAGATION SOURCE BASED ON LIBRARY

FIG. 20

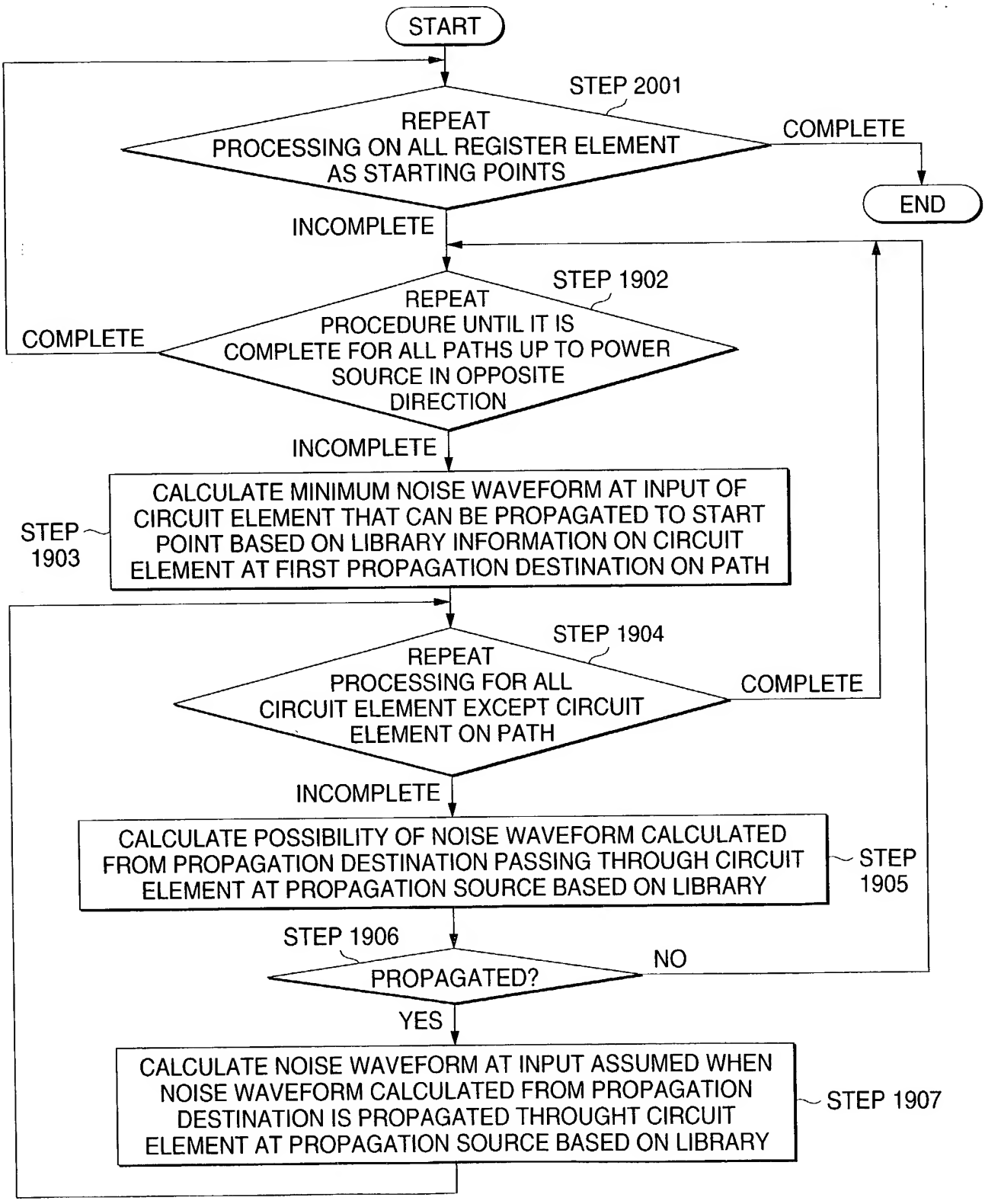
START
STEP 2001
REPEAT
PROCESSING ON ALL REGISTER ELEMENT
AS STARTING POINTS
COMPLETE
END
INCOMPLETE
STEP 1902
REPEAT
PROCEDURE UNTIL IT IS
COMPLETE FOR ALL PATHS UP TO POWER
SOURCE IN OPPOSITE
DIRECTION
COMPLETE
INCOMPLETE
STEP
1903
CALCULATE MINIMUM NOISE WAVEFORM AT INPUT OF
CIRCUIT ELEMENT THAT CAN BE PROPAGATED TO START
POINT BASED ON LIBRARY INFORMATION ON CIRCUIT
ELEMENT AT FIRST PROPAGATION DESTINATION ON PATH
STEP 1904
REPEAT
PROCESSING FOR ALL
CIRCUIT ELEMENT EXCEPT CIRCUIT
ELEMENT ON PATH
COMPLETE
INCOMPLETE
CALCULATE POSSIBILITY OF NOISE WAVEFORM CALCULATED
FROM PROPAGATION DESTINATION PASSING THROUGH CIRCUIT
ELEMENT AT PROPAGATION SOURCE BASED ON LIBRARY
STEP
1905
STEP 1906
PROPAGATED?
NO
YES
CALCULATE NOISE WAVEFORM AT INPUT ASSUMED WHEN
NOISE WAVEFORM CALCULATED FROM PROPAGATION
DESTINATION IS PROPAGATED THROUGHT CIRCUIT
ELEMENT AT PROPAGATION SOURCE BASED ON LIBRARY
STEP 1907

FIG. 21

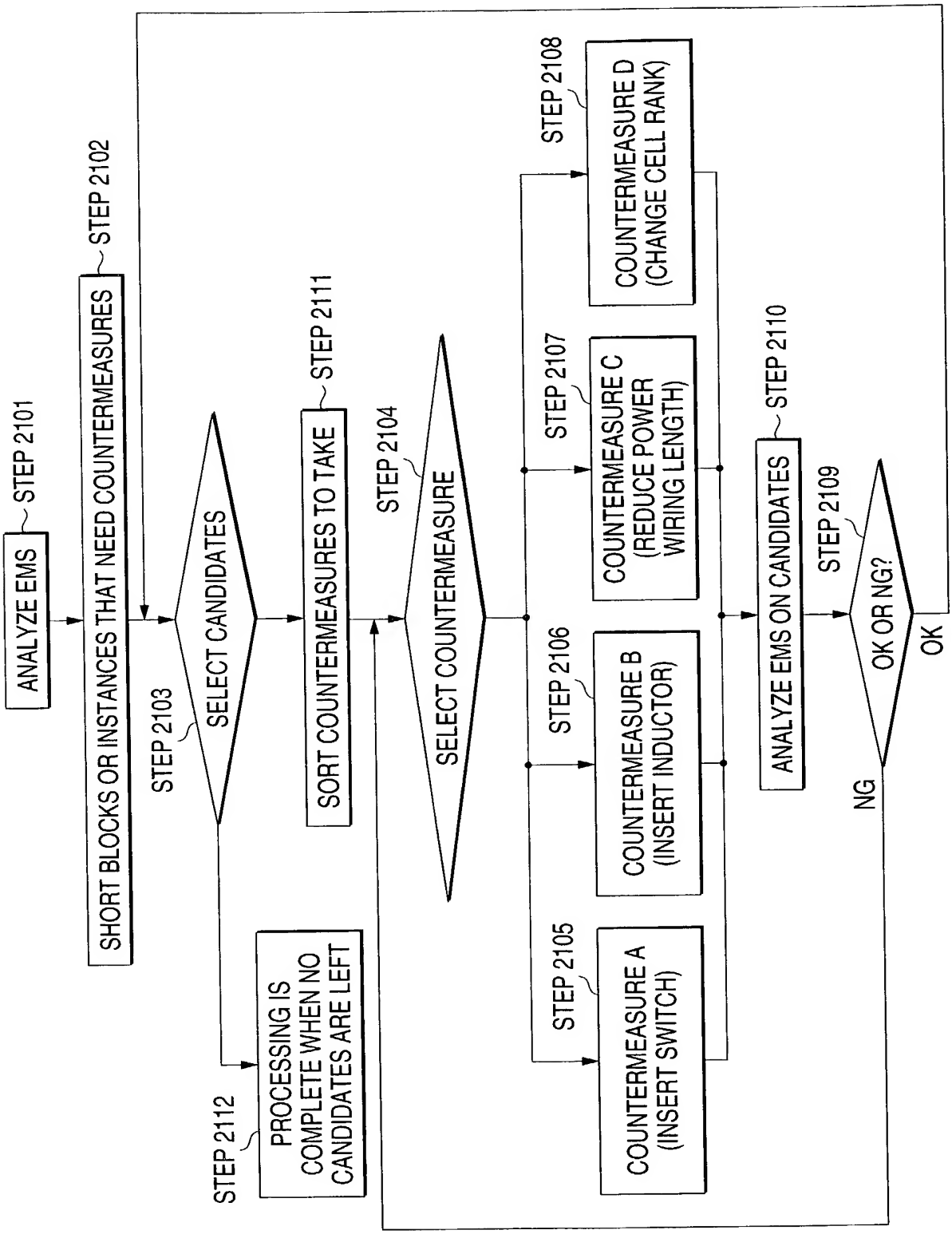
ANALYZE EMS
STEP 2101
SHORT BLOCKS OR INSTANCES THAT NEED COUNTERMEASURES
STEP 2102
SELECT CANDIDATES
STEP 2103
PROCESSING IS COMPLETE WHEN NO CANDIDATES ARE LEFT
STEP 2112
SORT COUNTERMEASURES TO TAKE
STEP 2111
SELECT COUNTERMEASURE
STEP 2104
COUNTERMEASURE A (INSERT SWITCH)
STEP 2105
COUNTERMEASURE B (INSERT INDUCTOR)
STEP 2106
COUNTERMEASURE C (REDUCE POWER WIRING LENGTH)
STEP 2107
COUNTERMEASURE D (CHANGE CELL RANK)
STEP 2108
ANALYZE EMS ON CANDIDATES
STEP 2110
OK OR NG?
STEP 2109
NG
OK

FIG. 22

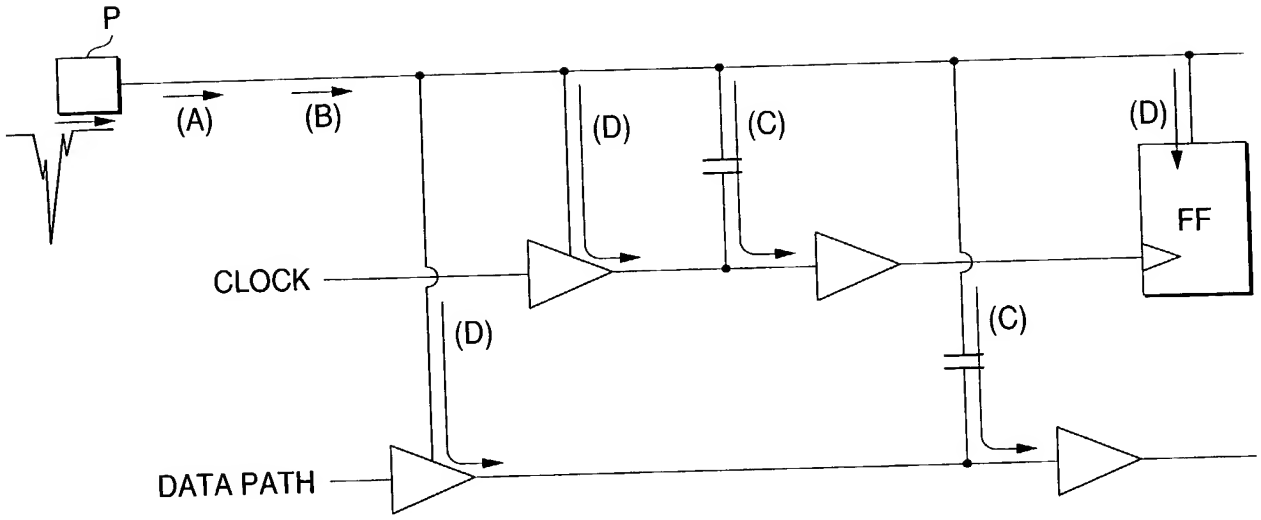

FIG. 23

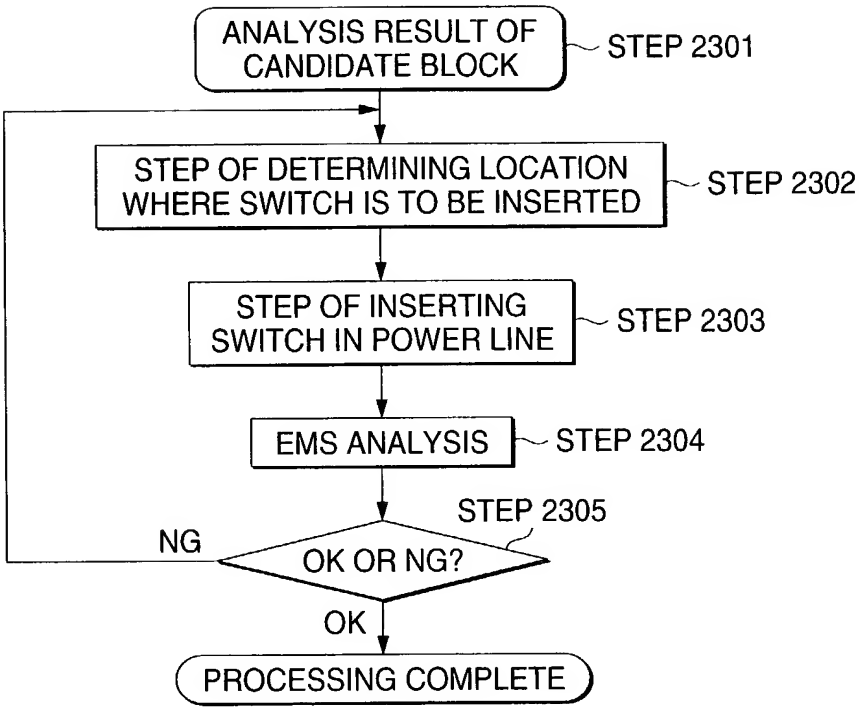
ANALYSIS RESULT OF CANDIDATE BLOCK
STEP 2301
STEP OF DETERMINING LOCATION WHERE SWITCH IS TO BE INSERTED
STEP 2302
STEP OF INSERTING SWITCH IN POWER LINE
STEP 2303
EMS ANALYSIS
STEP 2304
STEP 2305
NG
OK OR NG?
OK
PROCESSING COMPLETE

FIG. 24

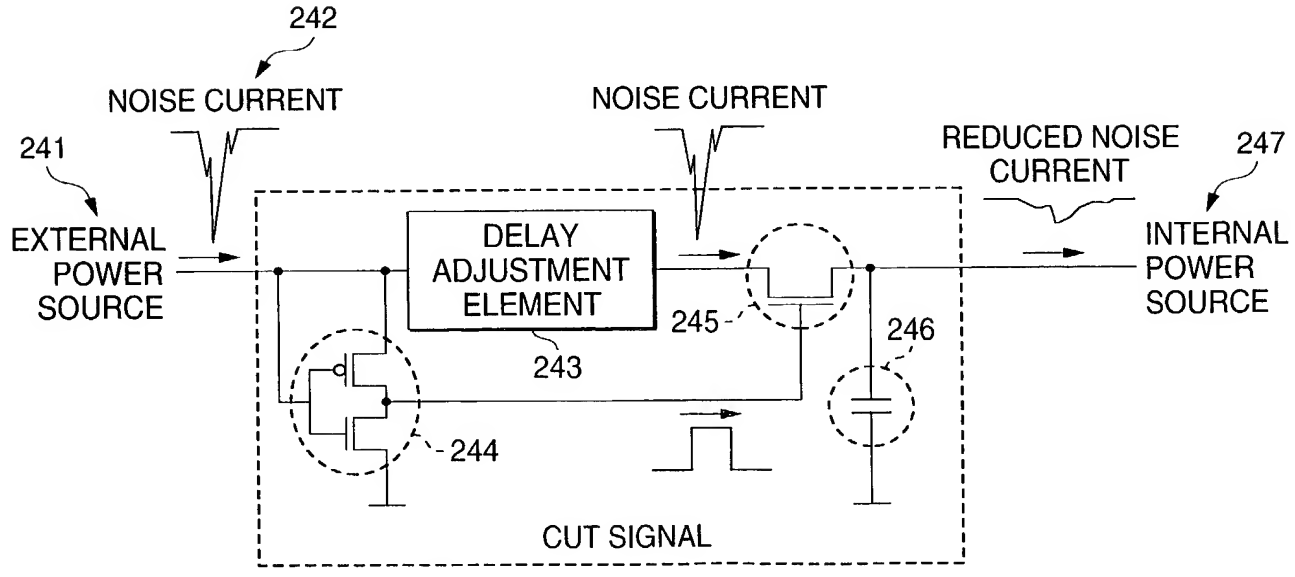
242
NOISE CURRENT
NOISE CURRENT
241
REDUCED NOISE CURRENT
247
EXTERNAL POWER SOURCE
DELAY ADJUSTMENT ELEMENT
INTERNAL POWER SOURCE
245
246
243
244
CUT SIGNAL

FIG. 25

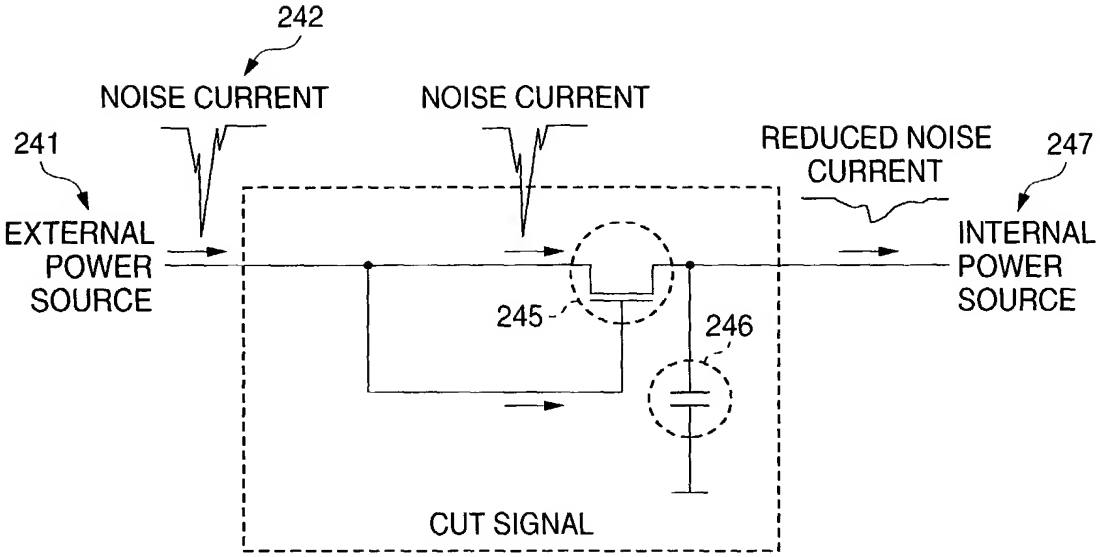
242
NOISE CURRENT
NOISE CURRENT
241
REDUCED NOISE CURRENT
247
EXTERNAL POWER SOURCE
INTERNAL POWER SOURCE
245
246
CUT SIGNAL

FIG. 26

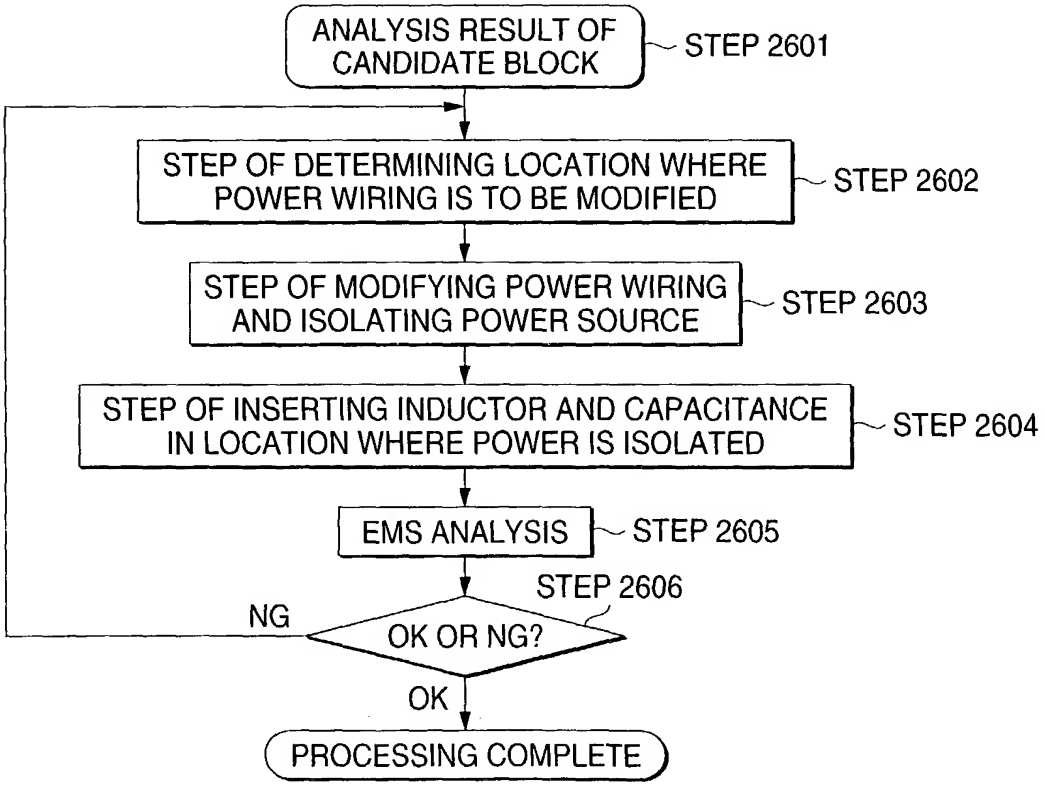
ANALYSIS RESULT OF CANDIDATE BLOCK
STEP 2601
STEP OF DETERMINING LOCATION WHERE POWER WIRING IS TO BE MODIFIED
STEP 2602
STEP OF MODIFYING POWER WIRING AND ISOLATING POWER SOURCE
STEP 2603
STEP OF INSERTING INDUCTOR AND CAPACITANCE IN LOCATION WHERE POWER IS ISOLATED
STEP 2604
EMS ANALYSIS
STEP 2605
STEP 2606
NG
OK OR NG?
OK
PROCESSING COMPLETE

FIG. 27

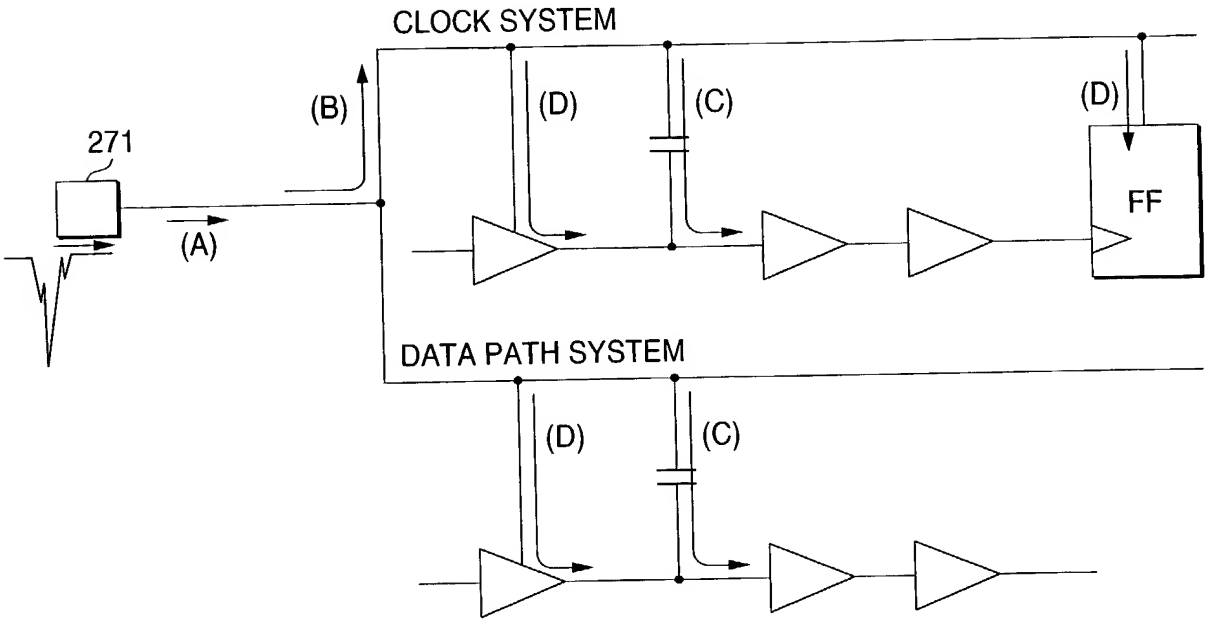
CLOCK SYSTEM
(B)
(D)
(C)
(D)
271
FF
(A)
DATA PATH SYSTEM
(D)
(C)

FIG. 28

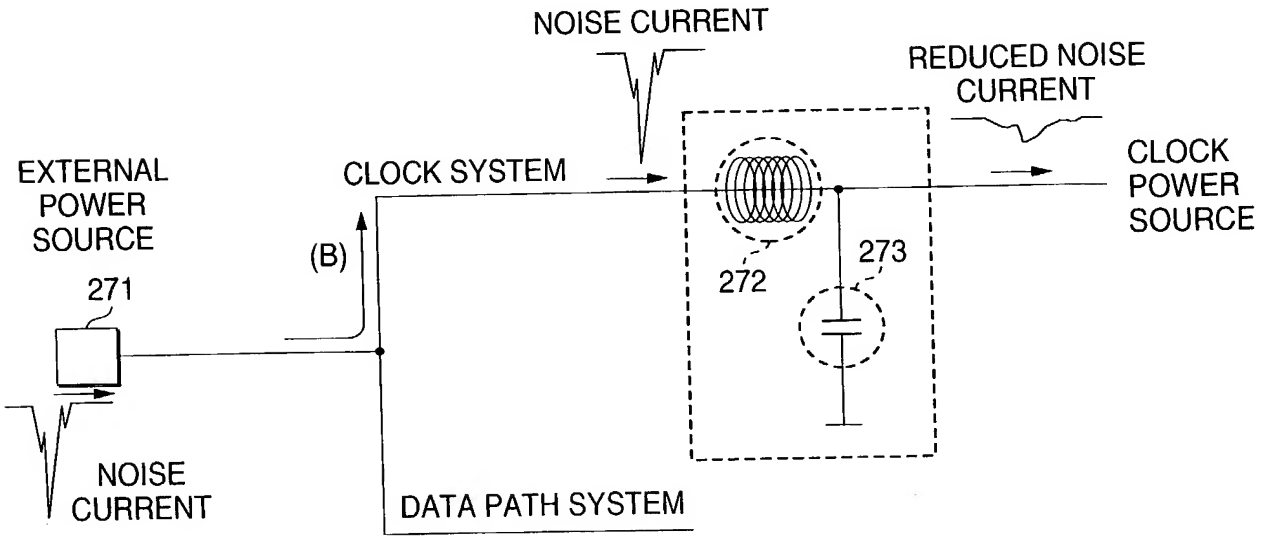
NOISE CURRENT
REDUCED NOISE CURRENT
EXTERNAL POWER SOURCE
CLOCK SYSTEM
CLOCK POWER SOURCE
(B)
272
273
271
NOISE CURRENT
DATA PATH SYSTEM

FIG. 29

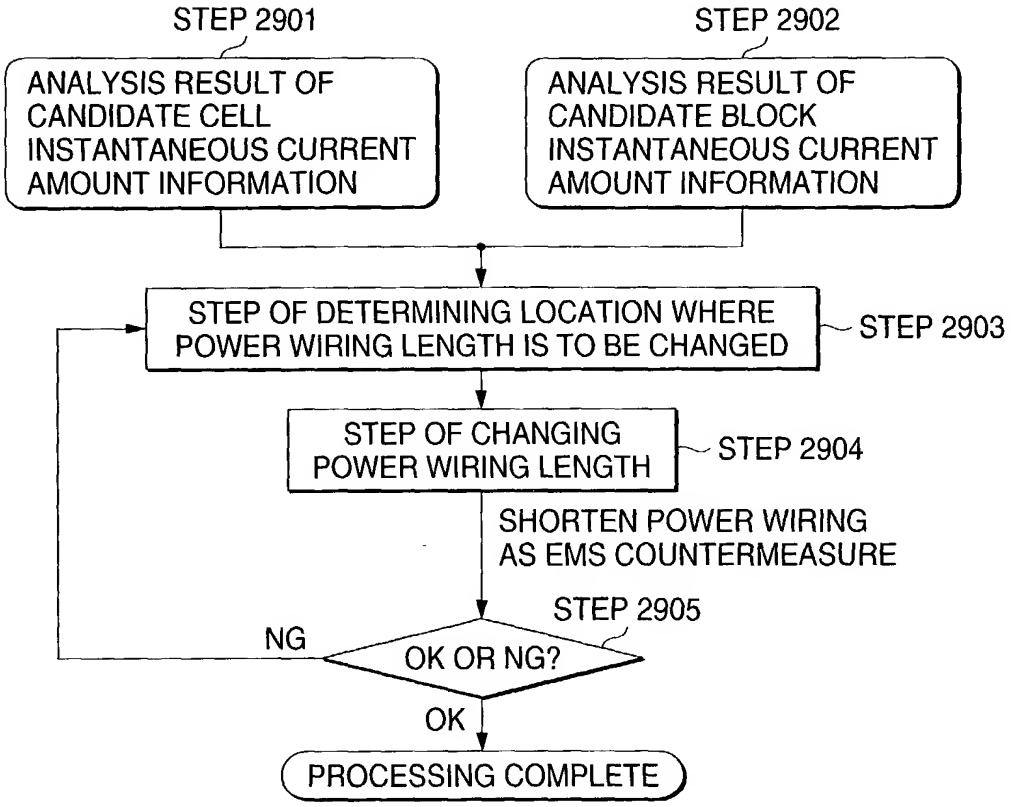
STEP 2901
ANALYSIS RESULT OF CANDIDATE CELL INSTANTANEOUS CURRENT AMOUNT INFORMATION
STEP 2902
ANALYSIS RESULT OF CANDIDATE BLOCK INSTANTANEOUS CURRENT AMOUNT INFORMATION
STEP OF DETERMINING LOCATION WHERE POWER WIRING LENGTH IS TO BE CHANGED
STEP 2903
STEP OF CHANGING POWER WIRING LENGTH
STEP 2904
SHORTEN POWER WIRING AS EMS COUNTERMEASURE
STEP 2905
NG
OK OR NG?
OK
PROCESSING COMPLETE

FIG. 30

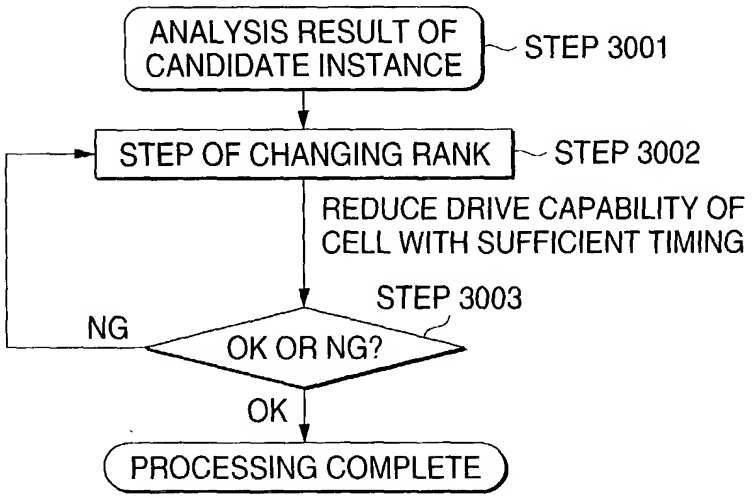
ANALYSIS RESULT OF CANDIDATE INSTANCE
STEP 3001
STEP OF CHANGING RANK
STEP 3002
REDUCE DRIVE CAPABILITY OF CELL WITH SUFFICIENT TIMING
STEP 3003
NG
OK OR NG?
OK
PROCESSING COMPLETE

FIG. 31

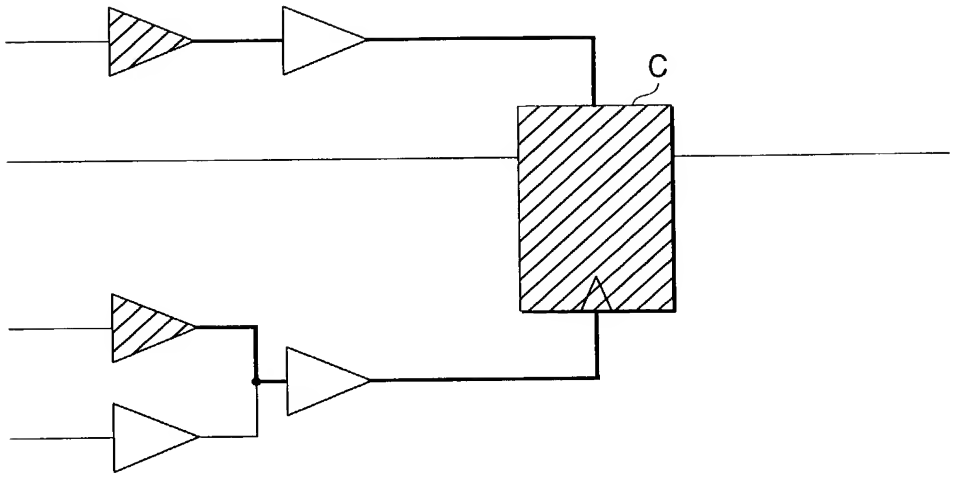

FIG. 32

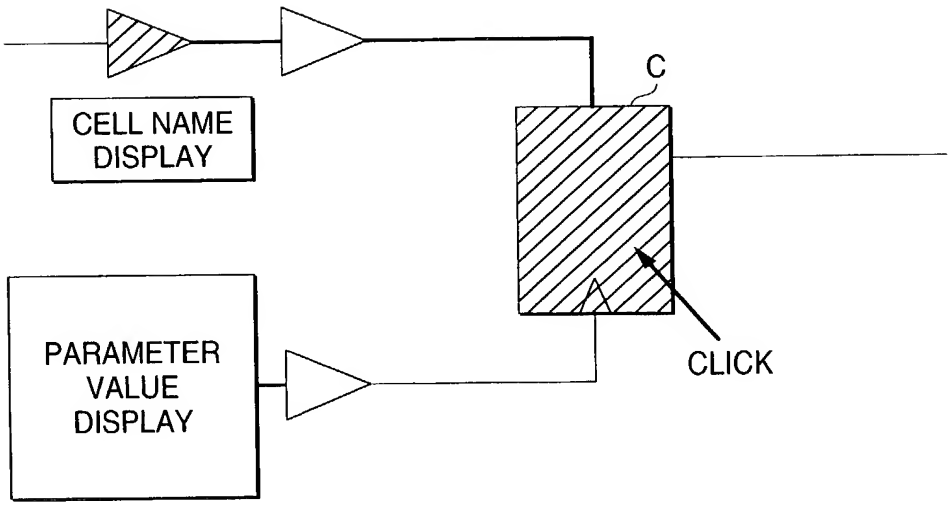

FIG. 33

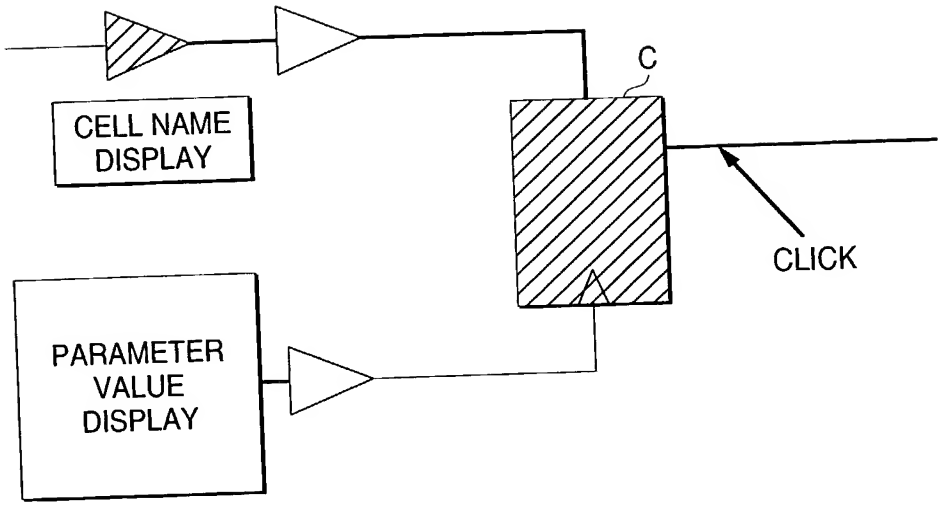
C
CELL NAME DISPLAY
CLICK
PARAMETER VALUE DISPLAY

FIG. 34

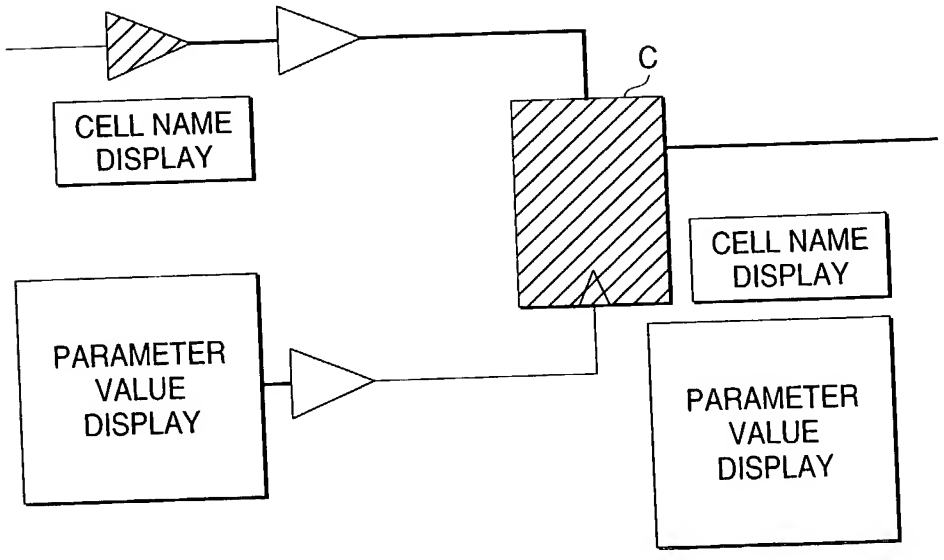
C
CELL NAME DISPLAY
CELL NAME DISPLAY
PARAMETER VALUE DISPLAY
PARAMETER VALUE DISPLAY

FIG. 35

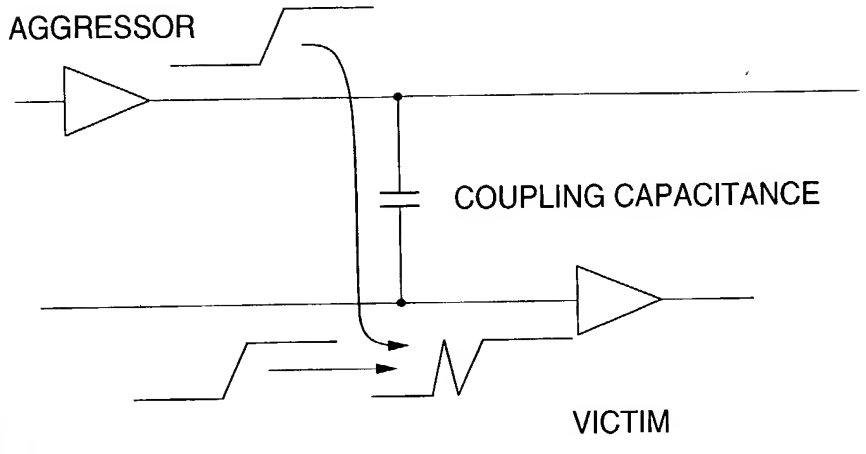

FIG. 36

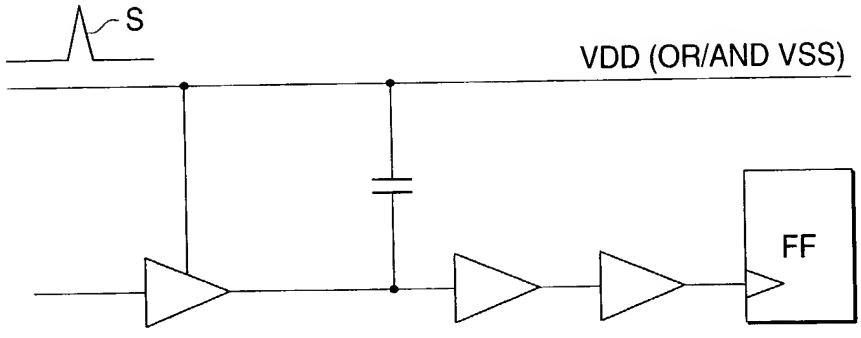

FIG. 37